EUROPEAN PATENT APPLICATION

(71) Applicant: International Business Machines
Corporation
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: Newton, Stephen Francis
134 Bean Hill Road
Endicott, New York 13760(US)
Inventor: Blocher, William Steven
8215 N Oracle Road
Tucson, Arizona 85704(US)
Inventor: Cassidy, Bruce Michael
898 Ponce de Leon Road
Boca Raton, Florida 33432(US)
Inventor: Groves, James Oliver, Jr.
187 East Campville Road
Endicott, New York 13760(US)
Inventor: Malik, Randhir Singh
2149 Marquesas Lane
Lexington, Kentucky 40509(US)

(74) Representative: Mönig, Anton, Dipl.-Ing.
IBM Deutschland Informationssysteme
GmbH,
Patentwesen und Urheberrecht
D-70548 Stuttgart (DE)

(54) Critically continuous boost converter.

(57) In critically continuous boost converters used to achieve high power factor and low input current harmonic distortion, a power FET is driven by a pulse generator whose on time is essentially constant over a single line cycle. Off time is terminated when current in the inductor falls to zero and the voltage on the side of the inductor not connected to the input voltage is less that the input voltage. A delay causes turn on to occur at the minimum of the voltage ring to minimize turn on switching losses. At voltages when the input voltage is less than one half of the output voltage part of the on time, turn on occurs with negative current flowing through the FET power switch and the inductor. Part of the turn on time is used to charge the inductor current back to zero before energy can begin to flow back into the output of the converter. A correction circuit is provided which extends the on time as a function of the input and output voltage to avoid dead time around the zero voltage crossover of the sinusoidal input voltage which when rectified provides the input voltage to the converter.
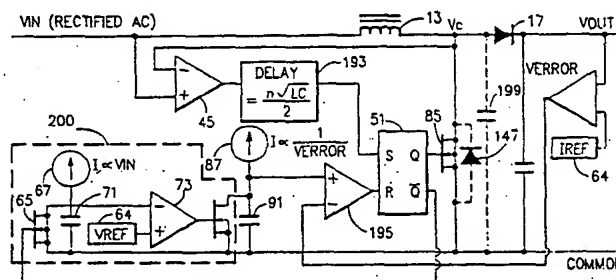
FIG.10

EP 0 582 813 A2

The present application is related to co-pending application SN/ 927,903 (Reference EN 992 089) entitled "Dropout Recovery Circuit" assigned to the same assignee as the present invention, and filed on the same date as the present application. The co-pending application is hereby incorporated by reference.

The present invention relates to boost converters and more particularly to continuous variable frequency boost converters.

Many conventional off line power supplies have input stages that contain a bridge rectifier followed by a large bulk capacitor. Such power supplies only draw current from the peak of the input line voltage waveform, when the input voltage is above the bulk voltage of the capacitor. The power factor of power supplies with bulk capacitors is low, reducing the amount of power that can be drawn from a source of a given volt ampere (VA) rating. The utility voltage waveforms are distorted by the excessive current drawn at the peak of the sinusoidal wave.

Power factor corrected power supplies place a circuit having a series inductor before the bulk capacitor. Usually this is a switching power supply circuit, often of the boost type. When a constant frequency, continuous conduction mode boost converter is used, input current is sensed with a resistor and duty cycle is adjusted to force the input current waveform to match the shape of the input voltage wave. The amplitude of the current is adjusted at a very slow rate to keep the voltage on the bulk capacitor approximately constant. Efficiency of this type of circuit is reduced by the power dissipated in the sense resistor, switching losses in the power switch, and reverse recovery current of the diode.

Switching the power switch of the boost converter when the inductor current is at a minimum minimizes switching losses in the transistor, transition losses, reverse recovery losses through the diode between boost inductor and output capacitor and common-mode noise. The current through the output diode of the boost converter or the voltage across the output diode is typically monitored to determine when inductor current is at a minimum. Sensing the current in the diode or the voltage across the diode introduces errors due to inductor ringing due to interaction of the inductance with circuit capacitances making accurate detection of zero current in the inductor difficult. Inaccurate detection of zero current results in transistor switching with increased diode recovery losses and transistor switching losses.

To reduce losses the boost converter can be operated in a critically continuous mode which occurs at the boundary between the continuous and discontinuous mode.

It is an object of the present invention to provide a critically continuous boost converter with accurate determination of zero current in the boost inductor without measuring inductor current.

It is another object of the present invention to provide a critically continuous boost converter which achieves near unity power factor.

It is still another object of the present invention to provide a critically continuous boost converter with reduced rectifying diode recovery loss and reduced switch capacitance loss.

It is a further object of the present invention to reduce crossover distortion in the current waveforms drawn by variable frequency, critically continuous high power factor switching power supplies.

In one aspect of the present invention a boost converter operating in a critically continuous mode having an input connectable to voltage source is provided. The boost converter includes an inductor and a power switch in series with the inductor. The series combination of the inductor and the power switch is connectable to the voltage source for receiving power therefrom. A rectifier means is connected between a load and the junction of the inductor and the power switch. The rectifier means is poled to conduct power to the load when the power switch is not conducting. Means for terminating the off time of the power switch is provided including means for monitoring the voltage across the inductor, means responsive to the monitored voltage for determining when the inductor voltage falls to zero, and delay means responsive to the inductor voltage falling to zero for introducing a delay sufficient to minimize the power switch turn on switching losses.

In another aspect of the present invention a critically continuous boost converter having an input coupled through a rectifier to a sinusoidal line voltage is provided. The boost converter includes an inductor and a power switch in series with the inductor. The series combination of the inductor and the power switch is connectable to a voltage source for receiving power therefrom. A rectifier means is connected between a load and the junction of the inductor and the power switch. The rectifier means is poled to conduct power to the load when the power switch is not conducting. Control loop means, responsive to a signal proportional to the output voltage of the load, is provided for controlling the on time of the power switch, the control means includes means for generating an error signal proportional to the difference of the signal proportional to the output voltage and a first reference voltage, first and second consecutive timing means, the first timing means for extending the the turn on of the power device and including means for generating a first signal proportional to

the input voltage, means for integrating the first signal, means for comparing the integrated signal to a second reference signal for starting operation of the second timing means for determining when the power switch on time ceases.

Ways of carrying out the invention are described in detail below with reference to drawings showing only specific embodiments in which:

Fig. 1
is a block diagram representation of a power system for supplying DC bus voltages for distributed power use by isolated DC/DC converters while drawing near in-phase sinusoidal input current from an AC supply line.

Fig. 2
is a part block diagram part schematic representation of the boost converter shown in Fig. 1.

Fig. 3
is a part schematic part block diagram of the application specific integrated circuit shown in Fig. 2.

Fig. 4
is schematic diagram representation of the square root block of Fig. 3.

Fig. 5
is a more detailed schematic representation of the circuit in Fig. 4.

Fig. 6
is a part schematic part block diagram representation of prior art timing circuitry to regulate the on and off times of the power switch used to control the power flow within the power supply.

Fig. 7
is a part schematic part bloc diagram representation of the timing circuitry in accordance with the present invention.

Fig. 8
is a part schematic part block diagram representation of a voltage regulating control loop for the boost converter of Figs. 2 and 3.

Fig. 9
is a waveform diagram of the inductor current and power switch on time.

Fig. 10
is a simplified block diagram of a critically continuous boost converter with a preregulator used to achieve high power factor and low harmonic distortion.

Fig. 11
shows the rectified line voltage waveform Vin(t) which is provided to the boost converter and the inductor current, whose average value follows the input voltage waveform to achieve high power factor and low input current harmonic distortion.

Figs. 12A and 12B
show inductor current and FET voltage, respectively, on a common time scale for high input

voltage conditions and Figs. 12C and 12D show inductor current and FET voltage, respectively, on a common time scale for low input voltage conditions.

Fig. 13
shows current distortion in the input current drawn from an AC power source due to LC resonance in the circuit.

Fig. 14
shows the effects of LC resonance on the inductor current causing negative current to flow when the input voltage is low.

Referring now to the drawing wherein like numerals indicate like elements throughout and particularly Fig. 1 thereof, a block diagram of a power system for supplying DC bus voltages for distributed power use by isolated DC/DC converters while drawing near in-phase sinusoidal input current from an AC supply line is shown. An electromagnetic interference (EMI) filter 1 is shown connected to an AC line protected by a fuse 2. A full wave rectifier bridge 3 receives the filtered AC line and provides a DC input to a boost (step-up) switchmode DC-DC converter 4. The DC output voltage, which is greater than the DC input voltage, is provided to one or more isolated DC/DC converters 5 which provide power to a load (not shown).

Referring to Fig. 2, the boost converter 4, including an application specific integrated circuit (ASIC) which serves as a controller 9 for the boost converter, is shown. The boost converter 4 comprises an input filter capacitor 11, an inductor 13, a power switch 15, a diode 17, and an output filter capacitor 21. The input capacitor 11 is connected across the input terminals 23 and 25, which provide rectified and EMI filtered AC power to the converter. The capacitor 11 is selected to have a value which will filter high frequencies, much greater than 120 Hertz, generated by the boost converter and not significantly distort the rectified AC power supplied to the converter. Inductor 13 is connected in series with one end of capacitor 11, the other end of capacitor 11 is connected to the common input and output terminal 25 of the converter. The power switch comprises an NMOS transistor 15, having its source and drain connected to the other end of inductor 13 and common input output terminal 25. Diode 17 is in series with inductor 13 and diode 17 is poled to deliver energy stored in inductor 13 to a DC output terminal 27. Output filter capacitor 21 is connected between terminals 27 and 25 and serves as the bulk capacitor, providing energy storage. The output filter capacitor is sized to have a larger capacitance than input capacitance 11.

A part schematic part block diagram of the controller 9 is shown in Fig. 3. The controller provides five functions: 1) power switch turn-on; 2) power switch turn-off; 3) output voltage regulator; 4)

control logic and driver; and 5) monitor and protection circuitry. Referring now to Figs. 2 and 3, the controller 9 receives a signal labelled DRAIN which is proportional to the voltage on the drain of the power switch 15 from a voltage divider shown in Fig. 2, including two resistors 41 and 43 connected between the drain and the common terminal 25. The resistors 41 and 43 each have a respective capacitor 42 and 44 in parallel. The impedances of capacitors 42 and 44 are proportional to the resistors 41 and 43 they are in parallel with. The signal from the voltage divider passes through a delay circuit comprising resistor 38 and capacitor 40. Resistor 38 connects the voltage divider signal to the DRAIN input, with the cathode of diode connected to the DRAIN input terminal. The capacitor is connected between the DRAIN and common terminal 25. Signals that interface between the ASIC and external circuitry are designated by names all in caps. The controller receives a signal LINE proportional to the line voltage, which is the rectified input voltage from a voltage divider comprising resistors 35 and 37 connected between terminals 25 and 27. These two signals LINE and DRAIN are connected to the noninverting and inverting terminals of a comparator 45 in the power switch turn-on circuitry. The output of comparator 45 is connected to one input of a two input OR gate 47. The output of OR gate 47 is connected to the set terminal of an RS flip flop 51. The Q output of the flip flop is connected through a driver 48 to the output of the controller labelled DRIVE which is connected to the gate of transistor 15 and through an inverting driver 49 to the output of the controller labelled DRIVENOT which is connected to transistor 52. The Q output is also connected to one input of a two input OR gate 53. The other input of OR gate 53 is connected to the reset input of RS flip flop 51. The output of OR gate 53 is connected to the gate of an NMOS transistor 55. A current source 57 is connected in series with the drain and source of transistor, with the source connected to ground. A signal labeled MAXOFF is provided by current source 57 and is connected to one end of a capacitor 61 shown in Fig. 2. The other end of capacitor 61 is connected to the common terminal 25. The signal MAXOFF is also connected to the noninverting input of a comparator 63. A voltage reference generated by the controller circuitry 64, VREF, is connected to the inverting input of comparator 63. VREF is connected to capacitor 66 which is external to the controller. The output of comparator 63 is connected to the other input of OR gate 47.

The power switch turn-off control comprises an NMOS transistor 65 having its drain connected to a current source 67. The gate of the transistor is connected to the Qbar output of the RS flip flop 51.

The source of transistor 65 is connected to ground.

A signal labelled CROSS is provided by current source 67 and is connected to one end of a capacitor 71 shown in Fig. 2. The other end of capacitor 71 is connected to the common terminal 25. The signal CROSS is also connected to the inverting input of a differential amplifier 73. The noninverting input of differential amplifier 73 is connected to VREF. An NMOS transistor 75 is in series with a current source 77. The gate of the transistor is connected to the Qbar output of RS flip flop 51. The source of transistor 75 is connected to ground. A signal labelled VTIME is provided by current source 77 and is connected to one end of a capacitor 81 shown in Fig. 2. The other end of capacitor 81 is connected to the common terminal 25. The signal VTIME is also connected to the inverting input of a comparator 83. The noninverting input of the comparator is connected a voltage reference generated by the control circuit. An NMOS transistor 85 is in series with diodes 84 and 86 and a current source 87. The drain of the transistor 85 is connected to the cathode of diode 86. The anode of diode 86 is connected to the cathode of diode 84. The gate of the transistor is connected to the output of differential amplifier 73. The source of the transistor is connected to ground. A signal labelled TON is provided by current source 87 and is connected to the anode of diode 84. Signal TON is also connected to one end of a capacitor 91 shown in Fig. 2. The other end of capacitor 91 is connected to the common terminal 25. The noninverting input of comparator 95 is connected between current source 87 and transistor 85. The output of comparator 95 is connected to one input of a three input OR gate 97. The output of comparator 83 provides another input to OR gate 97. The output of OR gate 97 is connected to the reset terminal of RS flip flop 51.

The voltage regulator portion of the controller comprises linear mode amplifier 101 which has a signal labelled REG connected to the inverting input of amplifier 101. The signal REG, provided by a voltage divider comprising resistors 103 and 105, is proportional to the output voltage of the converter. Resistors 103 and 105 are connected in series between terminals 27 and 25. An operational amplifier 107 has a voltage VREF generated by controller circuitry in block 64, connected to its inverting input terminal. The output of operational amplifier 107 is connected to the base of an npn transistor 111. The collector and emitter are connected in series with a current source 113. The output of the current source is connected to the noninverting input of operational amplifier 101. The emitter of the transistor is connected to ground. The output of current source 113 is also connected to a capacitor 115, with the voltage across the

capacitor providing the signal labelled SSTART. The drain of an NMOS transistor 117 is connected to the junction of the current source 113 and the collector of transistor 111.

The source of transistor 117 is connected to ground. The signal SSTART is connected to the noninverting input of linear mode amplifier 101.

The output of an inverter 121 is connected to the gate of an NMOS transistor 123. The source of an NMOS transistor 125 is connected to the drain of transistor 123. The source of transistor 123 is connected to ground. The junction of the drain and source of transistors 123 and 125 is connected to the noninverting input of operational amplifier 127. The inverting input is connected to voltage signal REG from the voltage divider comprising resistors 103 and 105. The output of operational amplifier 127 is connected to the gate of npn transistor 131. The emitter of transistor 131 is connected to ground and the collector is connected to the drain of transistor 117. The collector is also connected to the noninverting input of, linear mode error amplifier 101. The output of linear mode amplifier 101 is connected to one of the two inputs of square root block 133, which is shown in more detail in Fig. 4. The output off amplifier 101 also provides the signal COMP to one end feedback compensating series connected resistor 132 and capacitor 134. The other end of the series connected resistor and capacitor is connected to controller signal REG. Also connected to one of the inputs of the square root block is a voltage signal labelled VINRMS which is proportional to the rectified average input voltage. A voltage divider comprising two resistors 135 and 137 connected in series between the terminal 23 and 25. A capacitor 141 is connected in parallel with resistor 137, which has one end connected to terminal 25. The output of the square root block 133 is connected to the inverting input of comparator 95 and through a resistor 143 external to the controller to common terminal 25 of the converter. The signal provided by the square root circuit is labeled ERROR.

The protection circuitry includes an inverter 145 which is connected to a digital signal ONOFF which is supplied externally to the controller. A high digital input turns the converter on, a low level turns the converter off. If no input is provided the level remains high. The output of inverter 145 is connected to one input of a two input OR gate 147. The output of OR gate 147 is connected to the gate of transistor 117 and to the reset terminal of a RS flip flop 151, which serves as the over voltage latch. A signal OVLATCH which is proportional to the output voltage of the converter and obtained from a voltage divider comprising resistors 153, 155, and 157 which are connected in series between the terminals 27 and 25. The signal OV-

LATCH is obtained between resistors 155 and 157 and is connected to the non-inverting input of a comparator 161. A zener diode reference 162 is connected to the inverting input of comparator 161. The output of comparator 161 is connected to the set terminal of RS flip flop 151. The Q output of flip flop 151 is connected to one input of three input OR gate 163 and to one input of three input NOR gate 165. The output of OR gate 147 is connected to the second input of three input NOR gate 165. A signal UVOUT which is proportional to the output voltage of the converter is obtained from the voltage divider comprising resistors 153, 155, and 157, from between resistors 153 and 155. The signal UVOUT is connected to the inverting input of hysteretic comparator 167. A voltage VREF is connected to the noninverting input of comparator 167. The output of comparator 167 provides the third input to NOR gate 165. The output of NOR gate 165 provides the signal PORBAR which is connected through a resistor 171 to isolated DC/DC converters 5 shown in Fig. 1. A signal NOLINE is developed across capacitor 175 from a current source 177. The signal is connected at one end to the common terminal 25 and is connected at the other end to the noninverting terminal on a comparator 181 in the controller. A reference voltage VREF is connected to the inverting input of comparator 181. The output of comparator 181 is connected to the second input of three input OR gate 163. The output of OR gate 163 is connected to the inverter 121 and to the gate of transistor 125. The signal LINE is connected to the noninverting input of a differential amplifier 183. A reference voltage VREF is connected to the inverting input. The output of differential amplifier is connected to the gate of an n-channel MOSFET 185. The drain of the MOSFET is connected to the noninverting input of comparator 181 and the source is connected to ground.

Referring now to Fig. 4, a simplified schematic circuit diagram of square root block 133 is shown. The square root block 133 provides a current proportional to the ratio of the square root of a first input voltage divided by a second input voltage. In the simplified schematic, a first voltage V1 is connected through a resistor 201 to the base and collector of an npn transistor 203. The emitter of 203 is connected to ground. A first current source Iref is connected to three npn transistors 205, 207, and 209 which are connected in series with one another. Each of the transistors 205, 207, and 209 has its base connected to its collector, with the collector of 205 connected to the first current source, and the emitter of transistor 205 connected to the collector of transistor 207. The emitter of transistor 207 is connected to the collector of transistor 209. The emitter of transistor 209 is con-

nected to a second current source Iref which in turn is connected to ground. The collector of transistor 203 is connected to the emitter of transistor 209. Output current Io is connected to the collector of npn transistor 211. The collector of transistor 205 is connected to the base of transistor 211. The emitter of transistor 211 is connected to the collector of npn transistor 213. The base of transistor 213 is connected to its collector. The emitter of transistor 213 is connected to a current source Io which in turn is connected to ground. A voltage V2 is connected through a resistor 215 to the collector of an npn transistor 217. Transistor 217 is in series with an npn transistor 219. The base and collector of transistor 217 are connected to one another. The base and collector of transistor 219 are also connected to one another. The emitter of transistor 213 is connected the base of transistor 217 and the emitter of transistor 219 is connected to ground.

Operation of the simplified schematic, shown in Fig. 4, is as follows. The current in transistor 203 is approximately equal to VI divided by resistor 201, with the voltage across transistor 203 proportional to In (V1/R1) according to the Ebers-Moll equation. The current flowing into transistor 203 from transistor 209 is balanced by current flowing into the second current source Iref. Current Iref from the first current source flows through transistors 205, 207, and 209, so the voltage across the three devices is proportional to 3In(Iref). The voltage at the base of transistor 211 is therefore proportional to 3In(Iref)+In(V1/R1). The current in transistors 207 and 209 is approximately equal to V2/R2, so the voltage across transistors 217 and 219 is proportional to 2In(V2/R2). Current flowing into transistor 217 from the emitter of transistor 213 is balanced by current flowing into the Io source. The voltage across the base to emitter junctions of transistors 211 and 213 is shown by equation 1 below.

$$2\ln(Io) = 3\ln((Iref) + \ln(V1/R1) - 2\ln(V2/R2) \qquad (1)$$

Solving for Io results in equation 2, with Io being the current flowing in transistor 211.

$$Io = Iref^{1.5} \times ((V1/R1)^{0.5}) / (V2/R2)) \qquad (2)$$

Fig. 5 shows a circuit implementation of the simplified schematic of Fig. 4, in which the voltage drops across transistors 203, 217, and 219 are compensated for and the input bias current is reduced. Early voltage effects (where the base-to-emitter voltage varies slightly with collector-to-emitter voltage at a given collector current) are eliminated, and current cancellation circuits are implemented. Voltage V1 is connected to resistor 201 through a diode connected npn transistor 311. Diode con-

nected transistor 203 is in series with resistor 201 and the emitter of transistor 203 is connected to ground. The base of npn transistor 313 is connected to the base of transistor 203 and the emitter of transistor 313 is connected to the emitter of 203. Transistor 313 mirrors the current in transistor 203 and provides the mirrored current to a current mirror comprising pnp transistors 315 and 317. Transistor 315 and 317 have their emitters connected together and to a supply voltage. The base and collector of transistor 315 are connected to one another and to the collector of transistor 313. The current flowing through transistor 317 mirrors the current in transistor 315 and is provided to a diode connected npn transistor 321 which is in series with an pnp transistor 323 which has its collector connected to ground. The collectors of transistor 317 and 321 are connected together. The emitters of transistors 321 and 323 are connected together. The base of transistor 323 is connected to V1. An npn transistor 325 is in series with resistor 201, with the collector of transistor 325 connected to the emitter of transistor 317. The current through transistor 325 is controlled by the 2 Vbe drop across transistors 321 and 323 and provides a current in transistor 325 sufficient to make up for the voltage drop that occurs across transistor 203, so that V1 appears across 201 undiminished.

Similarly, the voltage drop that occurs across transistors 217 and 219 is compensated for by the current provided by npn transistor 345, which has its emitter connected to resistor 215 and its collector connected to the collector of transistor 325. Resistor 215 is in series with transistors 217 and 219. The base of transistor 345 is controlled by the voltage drop across series connected transistors 341, 343, 344 when the current through 217 and 219 is provided thereto by a current mirror comprising npn transistors 219 and 333, and a current mirror comprising pnp transistors 335 and 337. Current mirrors with pnp transistors source current while current mirrors with npn transistors sink current. Transistor 341 is an npn type while transistors 343 and 344 are pnp types. The base and collector of transistor 341 are connected to each other as is the base and collector of transistor 343. The collector of transistor 341 is connected to the collector of transistor 337 and to the base of transistor 345. The emitters of transistor 341 and 343 are connected to one another. The collector of transistor 344 is connected to the emitter of transistor 219. Voltage V2 is connected to the base of transistor 344. The bases and emitters of transistors 333 and 219 are connected to one another. The base and collector of transistor 335 are connected to one another and to the collector of transistor 333 and to the base of transistor 337.

A bias current provided to the base of pnp transistors 347, 349, and 351 which each have their emitters connected to one another and to supply voltage each provide a current Iref which is determined by the common bias current. Iref is supplied to series connected transistors 205, 207, and 209. A current mirror comprising npn transistors 353 and 355, has transistor 353 in series with transistor 209. Transistor 355 sets the current in the current mirror and the base of transistor 355 is connected to its collector, to the collector of transistor 349, and to the base of transistor 353. The emitter of transistors 353 and 355 are connected together and to a common voltage Vss. Therefore, transistor 353 carries Iref. To achieve a diode drop across transistors 211, 213, 217, and 219 to avoid the Early effect, transistor 356 which is in series with 211 and 213 provides sufficient current for the five Vbe drops across transistors 211, 213, 217, 219, and 331. The base voltage of transistor 357 is controlled by the voltage drop across series connected, npn transistors 357, 359, 361, 363, and 365, each of which has its collector connected to its base and carries the current Iref since the transistors are in series with transistor 351. The output current is supplied, by a current mirror which supplies current to two loads comprising pnp transistors 366, 367, 369, 371, with the current in transistor 367 controlling the current in transistors 369 and 371. A current mirror comprising npn transistors 373 and 375, with the current in transistor 375 controlling the current flowing in transistor 373, provides the current Io in series between 213 and ground. Transistor 377 eliminates the Early voltage effect in transistor 369. Transistor 371 of the current mirror provides the output Io of the circuit which represents a current proportional to the ratio of the square root of a first voltage V1 divided by a second voltage V2.

The operation of controller 9 when connected to a boost converter will now be described. When power switch 15 is turned on by controller 9, current in inductor 13 rises linearly from zero until the power switch is turned off. Diode 17 is reverse biased when the power switch is conducting, with the load current provided by capacitor 21. When the power switch is turned off, the voltage across the switch rises rapidly until diode 17 conducts, clamping the voltage across the switch to the output voltage level plus a diode drop. After all the energy in inductor 13 is expended, the voltage across the power switch begins to drop, as the Inductor rings with parasitic capacitances around the input voltage. The controller senses when the voltage has rung below the the input voltage and, after a delay to allow the voltage to reach its minimum value, switches on the power switch to initiate another operating cycle.

By allowing current in the inductor to drop to zero before turning the power switch on, switching losses associated with the diode's reverse recovery time are eliminated. Turning on the power switch when the voltage across it is at the minimum value of its ring excursion greatly reduces turn on switching losses. Turn off switching loss is reduced by turning the power switch off very rapidly, with the help of transistor 52, so that the power switch is off before parasitic capacitances have allowed voltage across it to rise significantly. Near unity power factor is obtained by maintaining the power switch on-time nearly constant over each AC line cycle, while adjusting the on-time at a slow rate to achieve output voltage regulation. The very slowly varying on time causes the current which is drawn from the power source to be proportional to the voltage across the inductor 13, which follows the rectified voltage waveform provided by the full wave rectifier bridge 3. When the current drawn by the boost converter is smoothed by the EMI filter 1 it results in a current waveform which is sinusoidal and in phase with the source sinusoidal voltage. A small correction to switch on-time is made each converter switching cycle to compensate for negative current flowing in inductor at the time the power switch is turned on. This correction is directly proportional to input line voltage.

Resistors 135 and 137, and capacitor 141 feed a voltage to controller 9 that is proportional to the average input line voltage. Resistors 35 and 37 feed a voltage to the controller that is proportional to the instantaneous line voltage. This is used to check for line outages, set current sources used to reduce current distortion and check for excessive volt time across inductor 13 preventing saturation. Capacitors 71 and 91 are used to set switch on-time. When power switch 15 is on, capacitor 71 is charged by a current proportional to the line voltage. When the voltage on capacitor 91 exceeds 1 volt, capacitor 91 is charged by a current from current source 87 inversely proportional to the error voltage. When voltage on capacitor 91 exceeds the error voltage, power switch 15 is turned off. While power switch 15 is still on, capacitor 81 is charged by a current from current source 77 proportional to the line voltage. If the voltage on capacitor 81 exceeds 5 volts, the power switch is turned off to prevent inductor 13 from saturating due to excessive volt time product. Capacitor 61 is charged by a constant current from current source 57 during the time the power switch is off. If the voltage on capacitor 61 exceeds 5 volts, the power switch is turned on. This prevents the converter from getting hung up in the off state due to situations where the normal turn-on circuit does not function. When the voltage on LINE is below 2.15 volts, capacitor 175 is charged by a constant current from current

source 177. If the voltage on capacitor 175 exceeds 5 volts, it is assumed that the input line voltage is not available and the converter does not switch the power switch 15. A circuit connected to SSTART is activated that causes the voltage on SSTART to track the voltage on REG, which is proportional to the output voltage of the converter, until the line voltage returns. When it returns, the converter restarts and the output ramps up to its nominal output voltage.

During start-up, capacitor 115 is charged by a constant current from zero to the nominal reference voltage by a constant current source 113. The controller adjusts the power switch on-time so that the voltage on REG is equal to the voltage on SSTART to achieve a soft start turn-on. If the controller is in shutdown mode, the voltage on SSTART is regulated to equal the voltage on REG. Resistors 153, 155, and 157 feed a voltage to the controller that is proportional to thee output voltage. If the voltage of UVOUT is below 5 volts, PORBAR is held low. Resistors 103 and 105 feed a voltage to the controller that is proportional to the output voltage. REG is the input to the controller's error amplifier 101. The output of error amplifier 101 appears on COMP, with resistor 132 and capacitor 134 providing feedback compensation. The square root of COMP voltage is divided by the voltage on INRMS to provide an error current on ERROR which is converted to a voltage by resistor 143. Resistors 41 and 43 and their respective parallel capacitors 42 and 44, provide a voltage to the controller that is proportional to the voltage across the power switch. When the voltage on DRAIN falls below the voltage on LINE, the power switch is turned on.

Switching power supplies usually employ timing circuitry to regulate the on and off times of the switches used to control the power flow within the supply. As shown in Fig. 6 labelled prior art, circuits often consist of a constant current source I charging a capacitor C to a predetermined level to set the switch on or off time. When the switch is turned on, a current source charges capacitor C. When the voltage on the capacitor exceeds an error voltage, Verror, a comparator output transitions terminating the power device on time and causing the voltage across the capacitor to be reduced to a low level. With previously employed timing circuitry the device on time is given by

$$TON = (C \times Verror)/I \quad (3)$$

If the input voltage is increased or the load decreased, it is often necessary to reduce the power device on time T to maintain regulation. As the on time is reduced, however, the timing circuitry becomes increasingly sensitive to noise. Since Verror

is so low, a small amount of noise will cause large proportional change in on time, with relationship expressed as

$$dT/T = (C)/(I)(T)) \cdot dVerror \quad (4)$$

Referring now to Fig. 8, a voltage regulating control loop for the boost converter of Figs. 2 and 3 is shown. Elements corresponding to elements shown in Figs. 2 and 3 have the same reference numerals. The control for the boost converter are designed so that FET 15 on time is effectively constant over one line (50/60 Hz)half-cycle and the power FET 15 is turned on almost immediately after the current in the inductor has decayed to zero from the previous switching cycle. This is illustrated in Fig. 9. A current source Iout provides an average current equal to the average output current of the boost converter operating on the continuous/discontinuous boundary.

$$Iout = (VINRMS)^2 (TON)/(2)(L)(Vout) \quad (5)$$

where TON is the power stage FET 15 on time, L is the power stage inductance 13, Vout is the average output voltage over one 50/60 Hz half-cycle, VINRMS is the rms value of the 50/60 Hz half-cycle. The power stage and controls provide Vout as an essentially DC voltage.

The average output voltage is developed across an impedance ZL representing the load impedance, connected across the current source Iout. The voltage is reduced by voltage divider comprising resistors 103 and 105 and supplied to operational amplifier 101 with resistor 132 and capacitor 134 providing feedback compensation. A voltage reference Vref1 is provided to the noninverting input of the operational amplifier 101 and corresponds to signal line 102 in Fig. 3. The output of the operational amplifier provides a voltage signal Vcomp, which is a function of the DC output current of the boost converter, to one input of square root block 133 which serves as a gain stabilizing stage. A signal proportional to the input voltage to the boost converter provides the other input to the gain stabilizing stage. The output of the gain stabilizing stage is a voltage signal ERROR together with the voltage across capacitor 91 in comparator 95 determines the duration of FET 15 on time.

Capacitor 91 is charged by a current inversely proportional to the voltage signal ERROR from current source 87, with the on time given by

$$TON = (TON/k2) (ERROR)^2 \quad (6)$$

The square root block provides

$$ERROR = k4 (COMP)^{1/2}/ k3 \, VINRMS \quad (7)$$

where k3 and k4 are constants.

The use of a charging current inversely proportional to the ERROR instead of a constant current reduces noise sensitivity. Since on time is proportional to the square of ERROR, a change in error voltage causes a proportionally larger change in on time compared to using a constant current source to charge the capacitor. This causes the circuit to be much less sensitive to noise, since the error voltage is higher for a comparable on time, a noise signal of a given amplitude causes a smaller proportional change in the on time. This can be expressed as

$$dT/T = 2(C/k2)^{1/2} \, dERROR \qquad (8)$$

Since sensitivity is a function of 1 over the square root of T rather than 1 over T which would occur if the charging current was constant sensitivity is reduced. For example, in a system with a maximum voltage one the capacitor of 4 volts running at 5% of the maximum on time, a 100 mvolt noise pulse would changed the on time by only 11% compared to a circuit which used a constant current source which would have a change in on time of 50%. This results in much less jitter in the circuit of the present invention. The open loop AC gain of the output voltage control loop Aol is

$$Aol = ZI(kj)(kk)(C_T(k4)^2/k2(k3)^2)(1/(2L(Vout)) \qquad (9)$$

where C_T corresponds to capacitor 91, $kj = R2/(R1+R2)$, and $kk = Z2/(Z1 + ((R1)(R2)/(R1+R2))$ and the AC gain is independent of the DC output current and VINRMS because of the use of the gain stabilizing stage.

Vout is held effectively constant by the control loop. Z1 can be easily be designed to be known in the region of thee open-loop unity gain crossover. Thus, the loop gain for all practical purposes is fixed by the values of the loop compensation components, all of which are fixed by the regulator designer. Without the gain stabilizing stage the open loop AC gain would vary with Vrms and with COMP which is a function of the DC output current. These loop gain variations make it impossible to fix the open loop unity gain bandwidth, which causes severe performance limitations when the loop compensation is set so that the regulator is stable for all COMP an VINRMS variations and has an acceptable maximum unity gain open loop gain over these variations.

Referring now to Fig. 10, a simplified block diagram of a critically continuous boost converter with a preregulator 193, used to achieve high power factor and low harmonic distortion is shown. The power FET 15 is driven by pulses provided by a comparator 195 responsive to the output voltage whose on time is essentially constant over a single line cycle. Off time is terminated when current in the inductor falls to zero and Vc falls below Vin(t). An additional delay provided in block 138, implemented in Fig. 2 by resistor 38 and capacitor 40, causes turn on to occur at the minimum of the voltage ring to minimize turn on switching losses. The waveform in Fig. 11 shows the rectified line voltage waveform present on Vin(t) and the inductor current, whose average value follows the input voltage waveform to achieve high power factor and low input current harmonic distortion.

When current in the inductor falls to zero, voltage on Vc rings down at a resonant frequency given by

$$F(res) = 2 \, pi \, (LC)^{1/2} \qquad (10)$$

where L is the inductance of the boost inductor and C is the parasitic FET and diode capacitance on node Vc, as well as any added external capacitance. Parasitic capacitance on node Vc, which appears across FET 85 is represented by capacitor 199 which shown connected in the circuit by dashed lines across the peak to voltage amplitude of the ring is 2(Vout-Vin(t)). If Vin(t) is more than half Vout, the control circuit turns the power FET on when the voltage on Vc is at its minimum value and the current in L is zero. If Vin(t) is less than half Vout, Vc is clamped at zero by the internal FET diode 197 prior to the turn on of the power FET. In this case, turn on occurs with negative current flowing through the FET and inductor. Part of the FET on time is therefore used to charge the inductor current back to zero before energy can begin to flow back into the converter. Figs. 12A and 12B show inductor current and capacitor voltage on node Vc, respectively, for high input voltage conditions and Figs. 12C and 12D show Inductor current and capacitor voltage, respectively, for low input voltage conditions. At very low input voltage, no net current flows in the converter, since the entire on time is required to return the inductor current to zero, then charge C back up to Vout. The result of this is a narrowing of the input current conduction angle with an on time dead time dependent around the zero voltage crossover of the input voltage as shown in Fig. 13.

The following equations show the value of the voltage at node Vc and inductor current, respectively, during the ringing, assuming current in L drops to zero at t = 0.

$$Vc(t) = (Vout-Vin(t)) \cos(1/(LC)^{1/2})t + Vin(t) \qquad (11)$$

$$Il(t) = -(C/L)^{1/2} (Vout-Vin(t)) \sin(1/(LC)^{1/2})t \qquad (12)$$

for Vc(t) > 0

Equation 13 gives the time at which the voltage at node Vc falls to zero in the condition when Vin(t) < 1/2 Vout.

$$t_{Vc=0} = (LC)^{1/2} \cos^{-1}(Vin(t)/(Vin(t)-Vout)) \qquad (13)$$

Equations 14 and 15 give different expressions for the inductor current when the voltage at node Vc reaches zero.

$$Il_{Vc=0} = -(C/L)^{1/2}(Vout-Vin(t))\sin(\cos^{-1}(Vin(t)/(Vin(t)-Vout))) \qquad (14)$$

$$Il_{Vc=0)} = (C/L)^{1/2} (Vout^2 - 2\,Vin(t)\,Vout)^{1/2} \qquad (15)$$

The crossover distortion can be reduced by adding a period of time to the FET on time to allow the inductor current to rise to zero before the normal "constant" on time period begins. This correction is accomplished by crossover correction circuitry 200. An exact expression for the amount of the time required for the current to reach zero is shown in equation 16. The inductor current versus time is shown in Fig. 14.

$$t_{correct} = (LC)^{1/2}/Vin(t) (Vout^2 - 2\,Vin(t)\,Vout)^{1/2} \qquad (16)$$

The expression in equation 16 will be negligibly small when Vin(t) is large, and can be approximated by equation 17. Likewise, the small time constant associated with this term at high line voltage will usually produce negligible error when Vin(t) > 1/2 Vout, even though no correction is called for under this condition.

$$t_{correct} = ((LC)^{1/2} Vo) / Vin(t) \quad \text{For Vin(t) small} \qquad (17)$$

The delay is introduced by current source 67 which has a current proportional to the average input voltage charging capacitor 71. Capacitor 71 is selected so that it is proportional to $((LC)^2 \, Vo)$. Comparator 73 determines when the appropriate delay occurs allowing current source 87 to charge capacitor 91.

Referring now to Fig. 2 and Fig. 3, the ASIC is divided into five sections: power switch turn on control; power switch turn off control; output voltage regulator; control logic and driver; and monitor and protection circuitry. The turn on circuitry functions as follows. When the voltage on DRAIN falls below the voltage on LINE, the output of comparator 45 goes high. This transition activates the SET input of flip flop 51 causing the Q output of flip flop 51 to transition high, which causes DRIVE to go high. When DRIVE goes high, the power switch 15 is turned on. The DRIVE line can alternatively be transitioned high by the voltage of MAXOFF exceeding a reference voltage VREF as determined in comparator 63. When DRIVE is high indicating that the power switch is on, or the output of OR gate 53 is high indicating the converter is shut down or the power switch is being shut off, OR gate 53 turns on transistor 55 which holds MAXOFF low. When the output of OR gate is low and therefor the switch is off, constant current source 57 causes the voltage on MAXOFF to increase by charging capacitor 61, and if MAXOFF exceeds VREF switch 15 is turned on.

Turn off can occur due to either of two conditions. During the time the power switch is off, the Qbar output of flip flop 51 causes transistor 65 and 75 to hold VTIME and CROSS low. Since the voltage on CROSS is below 1 volt, differential amplifier 73 causes transistor 85 to hold TON low, also. When the power switch is turned on, transistors 65 and 75 are turned off, so VTIME is charged by current source 77, and CROSS is charged by current source 67. Currents in both current sources are directly proportional to the voltage on LINE, so higher rectified input voltages causes capacitors 71 and 81 tied to VTIME and CROSS to charge at a faster rate. When the voltage on CROSS exceeds 1 volt, differential amplifier 73 turns off transistor 85, allowing voltage on external capacitor 91 tied to TON to rise. Capacitor 91 is charged by a current inversely proportional to the error voltage developed by linear mode amplifier 101. When voltage on TON exceeds ERROR voltage, comparator 95 causes an input to OR gate 97 to go high, triggering the reset input of flip flop 51, turning off the power switch 15. As the ERROR voltage increases, the current charging TON decreases, and the comparator threshold voltage increases, so a very large range of power switch on time can be produced. Alternatively, if the voltage on VTIME exceeds REF, comparator 83 causes an input to OR gate 97 to go high, again resetting flip flop 51 and turning off the power switch.

During light load conditions, the diodes 84 and 86 allow the voltage of the signal ERROR to go below the voltage of signal TON causing long off times between groups of several on off cycles. This condition is called burst operation. This is not a separate control scheme that is called upon the detection of certain events, but rather is part of the single control scheme that is used.

The voltage regulator portion includes soft start, gain compensation, and error amplifier circuitry. If ONOFF is low, or if the Vcc voltage monitor signals that the Vcc voltage is low, OR gate 147 causes OR gate 163 to hold SSTART low. When transistor 117 is turned off current source

113 charges an external capacitor 115 tied to SSTART with a constant current until the voltage on SSTART equals REF. At this point, operational amplifier 107 and transistor 111 control SSTART to equal Vref, assuming the controller is not shut down. If the controller shuts down, transistor 125 is turned on and transistor 123 is turned off, so operational amplifier 127 and transistor 131 regulate SSTART to equal REG. When the controller is not shut down transistor is off and transistor 123 is on with operational amplifier 127 having a zero voltage input provided to its noninverting input and therefor does not regulate the SSTART voltage. Amplifier 101 is the controller's error amplifier and it adjusts the voltage signal COMP so that the voltage REG equals the voltage on SSTART. Amplifier 101 is also the system error amplifier, with the output frequency compensated by resistor 132 and capacitor 134 and connected to REG. The square root circuit modifies COMP, the output of amplifier 101 to compensate for variations in gain due to load and input voltage. The square root of the COMP voltage is divided by the average value of the input voltage VINRMS to produce a current for generating the ERROR voltage signal.

OR gate 97 combines turnoff signals due to shutdown, excess volt time, and normal on time termination to produce a reset signal to flip flop 51. Flip flop 51 is set by OR gate 47.

The monitor and protection circuitry produces two outputs: a shut down line that holds the converter off, and a PORBAR line that powers an external device to short out the inrush limiting resistor. The PORBAR line can also be used to turn on and off cascaded converter stages. A low logical level on ONOFF or a high output from the Vcc voltage monitor produces a high output from gate 147, holding the shutdown line high, the PORBAR line low, and resetting over voltage latch 151. A high output from over voltage comparator 167, indicating the OVLATCH exceeds REF, latches 151, sending the shutdown line high, and the POR-BAR signal low. If the the voltage on UVOUT exceeds REF, the output of comparator 167 goes low, allowing PORBAR signal to go high. Voltage on UVOUT must fall below 1/2 REF signal before the PORBAR signal is switched low. If the LINE signal is above 2.15 volts, comparator 183 causes MOSFET 185 to hold NOLINE low. When the LINE signal goes low, an external capacitor tied to the NOLINE signal is charged by constant current source 177. If the voltage on the NOLINE signal exceeds the REF signal, the output of comparator 181 goes high, causing the converter to shut down. Gate 163 combines signals from the no line, over voltage latch 151, the Vcc voltage monitor and ONOFF circuits to produce the shut down signal. Gate 165 combines signals from the low output

voltage detector, over voltage latch, the ONOFF signal, and the Vcc voltage monitor to produce the PORBAR output.

The foregoing has described a circuit to reduce crossover distortion in the current waveforms drawn by variable frequency, critically continuous high power factor switching power supplies.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein with out departing from the spirit and scope of the invention.

Claims

1. A boost converter operating in a critically continuous mode having an input connectable to voltage source, comprising:
   an inductor;
   a power switch in series with said inductor, the series combination connectable to the voltage source for receiving power therefrom;
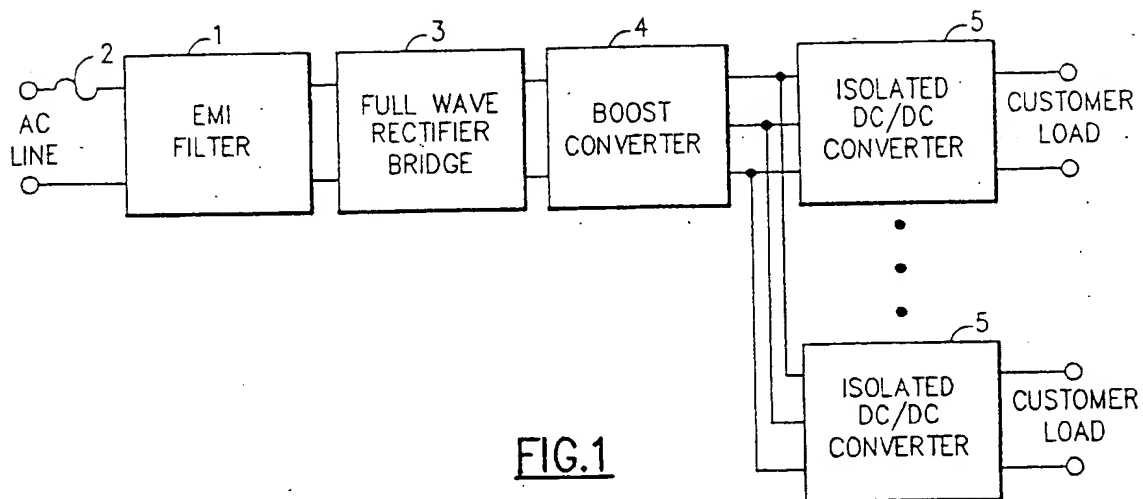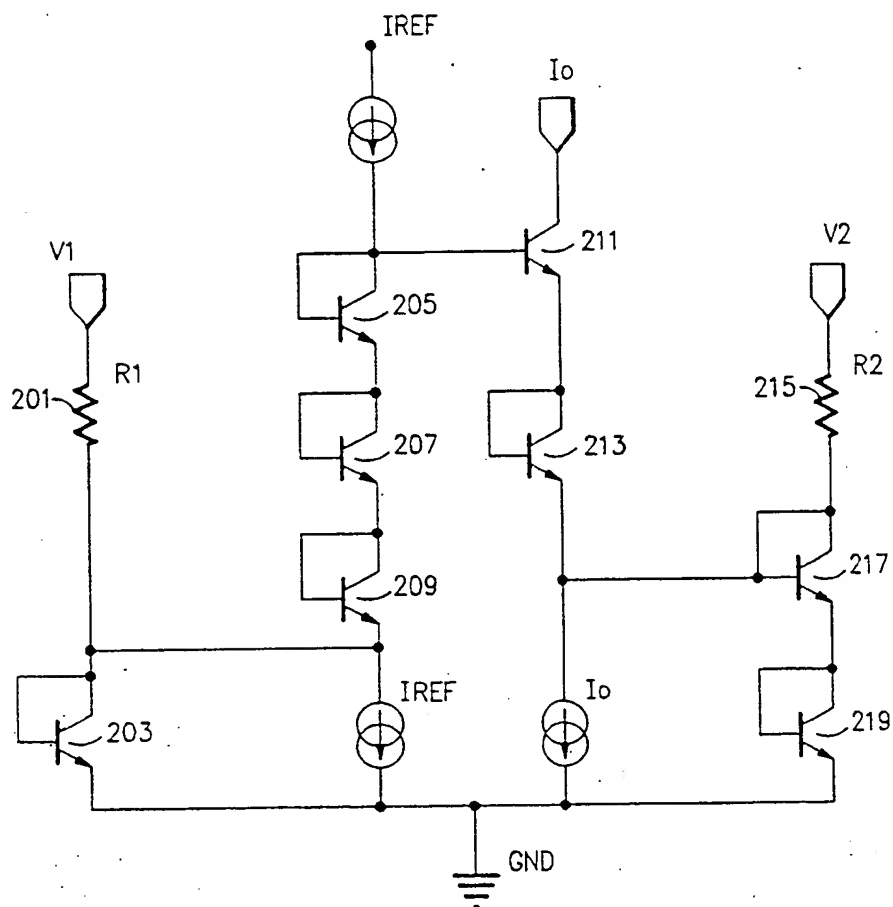   a rectifier means connected between a load and the junction of said inductor and said power switch, said rectifier means poled to conduct power to said load when said power switch is not conducting; and
   means for terminating the off time of said power switch including means for monitoring the voltage across the inductor, means responsive to the monitored voltage for determining when said inductor voltage falls to zero, and delay means responsive to said inductor voltage falling to zero for introducing a delay sufficient to minimize the power switch turn on switching losses.

2. The boost converter of claim 1 wherein said delay means provides a delay proportional to pi times the square root of L times C, where L is the inductance of the inductor and C is the parasitic and external capacitance across the power switch.

3. The boost converter of claim 1 or 2 wherein the on time of the power switch varies slowly compared to the switching rate of the power switch.

4. The boost converter of any one of the preceding claims 1 to 3 wherein said voltage source is obtained by rectifying a sinusoidal line voltage.

5. A critically continuous boost converter having an input connectable through a rectifier to a sinusoidal line voltage, said converter compris-

ing:

an inductor;

a power switch in series with said inductor, the series combination coupled to the line voltage for receiving power therefrom;

a rectifier means connected between a load and the junction of said inductor and said power switch, said rectifier means-poled to conduct power to said load when said power switch is not conducting;

control loop means, responsive to a signal proportional to the output voltage of the load, for controlling the on time of said power switch, said control means including means for generating an error signal proportional to the difference of said signal proportional to the output voltage and a first reference voltage, first and second consecutive timing means, said first timing means for extending the turn on time of said power device, said first timing means including means for generating a first signal proportional to the input voltage, means for integrating said first signal, means for comparing said integrated signal to a second reference signals for starting operation of said second timing means for determining when said power switch on time ceases.

6. The converter of claim 5, wherein said second timing means comprises means for integrating a signal which is a function of the difference of the output voltage from a desired value.

7. The converter of claim 5 or 6, further comprising means for introducing a delay after the current in the inductor current falls to zero and the voltage on the side of the inductor not connected to the input voltage is less than the input voltage for causing turn on to occur at the minimum of the voltage ring of the inductor.

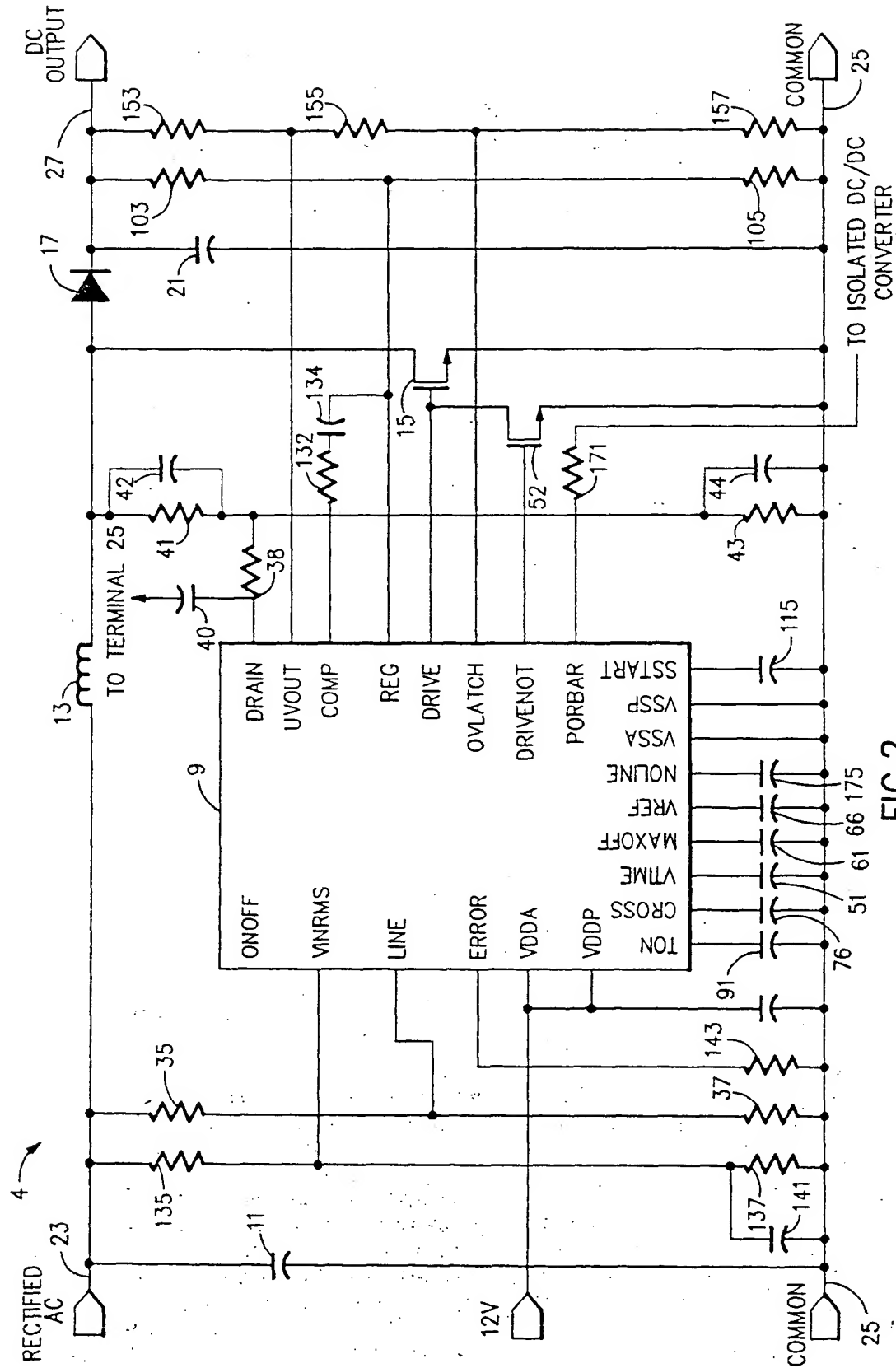8. A boost converter having an input connectable to a voltage source, comprising:

an inductor;

a power switch in series with said inductor, the series combination connectable to the voltage source for receiving power therefrom;

a rectifier means connected between a load and the junction of said inductor and said power switch, said rectifier means poled to conduct power to said load when said power switch is not conducting;

control loop means, responsive to a signal proportional to the output voltage of the load, for controlling the on time of said power switch, said control means including means for generating a compensating voltage signal from

a comparison of said signal proportional to the output voltage and a first reference voltage, means for generating an error signal proportional to the square root of said compensation signal and inversely proportional to the input voltage, timing means for generating a signal inversely proportional to said error signal, means for integrating said signal, means for comparing said integrated signal to a second reference signal for turning off said power switch when said second reference signal is exceeded, whereby the open loop gain of the control loop is independent of the boost converter DC output current and the boost converter input voltage.

9. The converter of claim 8, wherein said second timing means comprises means for integrating a signal which is a function of the difference of the output voltage from a desired value.

10. The converter of claim 8, further comprising means for introducing a delay after the current in the inductor falls to zero and the voltage on the side of the inductor not connected to the input voltage is less than the input voltage for causing turn on to occur at the minimum of the voltage ring of the inductor.
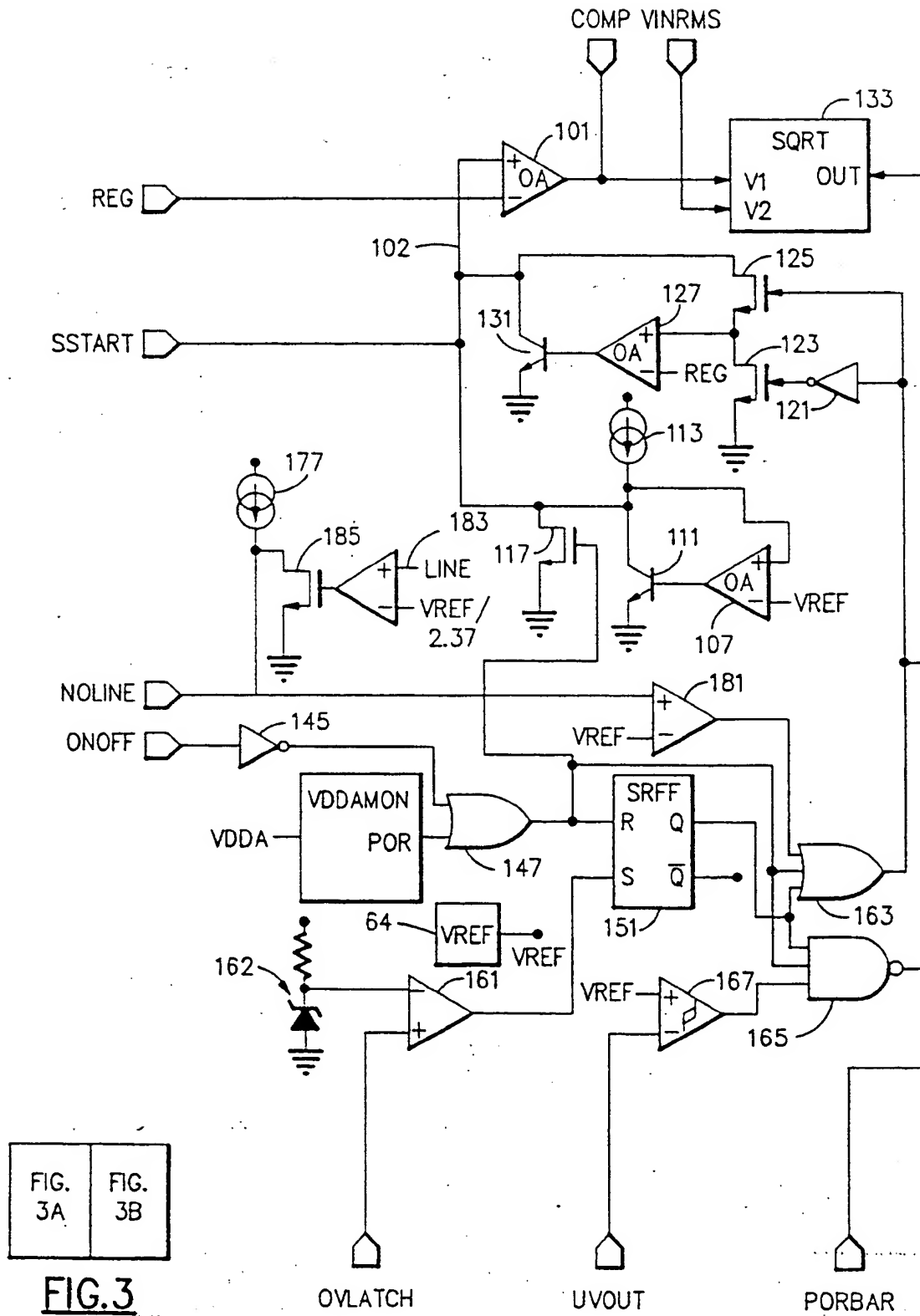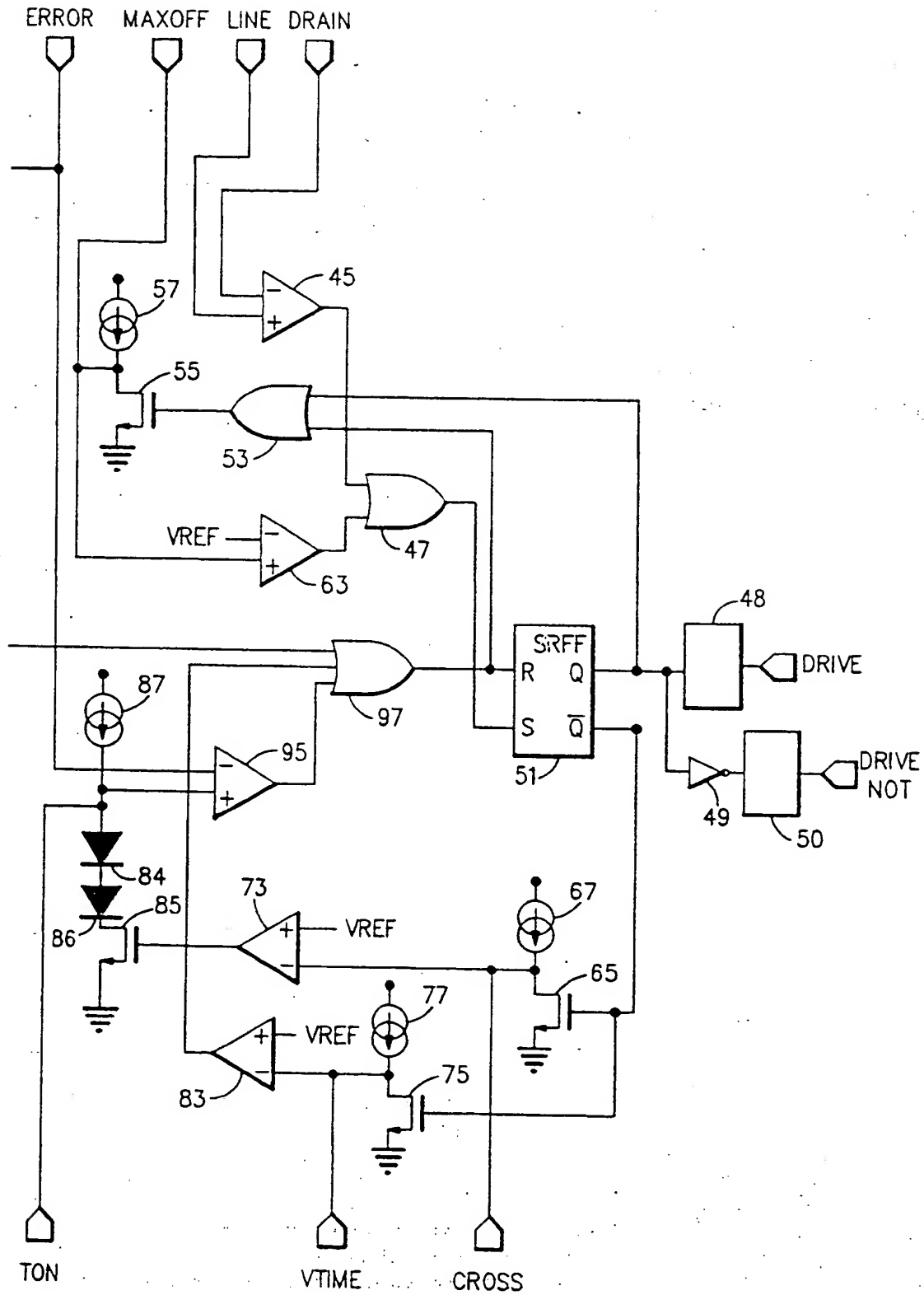
FIG.1

FIG.4

FIG.2

FIG.3A

ERROR   MAXOFF   LINE   DRAIN

57

45

55

53

VREF   63

47

SRFF
48

87

95

97

R   Q   DRIVE

S   Q̄

51   49   50   DRIVE NOT

84

85

73   VREF   67

86   65

83   VREF   77

75

TON   VTIME   CROSS

FIG.3B

FIG.5

FIG.6

Prior Art

FIG.7

VOUT

R1

REG

Z2

101

COMP

133

ERROR

IOUT
ZL
R2

ZI

–
+

GAIN
STABILIZING
STAGE

95

POWER
STAGE

IOUT

VREF

K_3 VRMSIN

TON

87

$\frac{K2}{ERROR}$

91

85

FIG.8

INDUCTOR CURRENT

TON

TIME

FIG.9

VIN (RECTIFIED AC)

13 Vc

17

VOUT

–
+

DELAY
= $\frac{n\sqrt{LC}}{2}$

193

199

VERROR

45

200

$I \propto \frac{1}{VERROR}$

51

85

147

IREF

64

$I \propto VIN$

87

+
–

S   Q

65
67

71

73

64
VREF

+
–

91

+
–

R   \overline{Q}

195

IREF

64

COMMON

FIG.10

FIG.11

FIG.13

INPUT
CURRENT

TIME

INDUCTOR
CURRENT

$$SLOPE = \frac{VOUT - VIN}{L}$$

$$SLOPE = \frac{VIN}{L}$$

TIME

$$T_{CORRECT} \cong \frac{\sqrt{LC} \; VOUT}{VIN}$$

FIG.14

INDUCTOR
CURRENT

TIME

FIG.12B

FET
VOLTAGE

TIME

FIG.12D

INDUCTOR
CURRENT

TIME

FIG.12A

FET
VOLTAGE

TIME

FIG.12C

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
	* Page 2, lines 26-46; fig.; claims 1,2 * ----		

DOCUMENTS CONSIDERED TO BE RELEVANT

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	11-10-1994.	MEHLMAUER

EPO FORM 1503 03.82 (P0401)

EUROPEAN PATENT APPLICATION

(71) Applicant: International Business Machines
Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor: Newton, Stephen Francis
134 Bean Hill Road
Endicott, New York 13760 (US)

Inventor: Blocher, William Steven
8215 N Oracle Road
Tucson, Arizona 85704 (US)
Inventor: Cassidy, Bruce Michael
898 Ponce de Leon Road
Boca Raton, Florida 33432 (US)
Inventor: Groves, James Oliver, Jr.
187 East Campville Road
Endicott, New York 13760 (US)
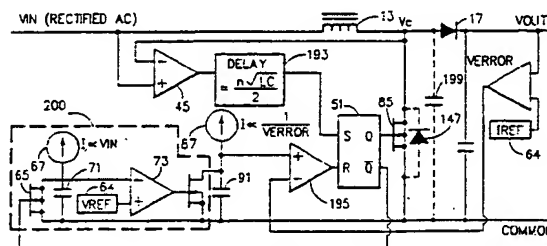Inventor: Malik, Randhir Singh
2149 Marquesas Lane
Lexington, Kentucky 40509 (US)

(74) Representative: Schäfer, Wolfgang, Dipl.-Ing.
IBM Deutschland Informationssysteme
GmbH
Patentwesen und Urheberrecht
D-70548 Stuttgart (DE)

(54) Critically continuous boost converter.

(57) In critically continuous boost converters used to achieve high power factor and low input current harmonic distortion, a power FET is driven by a pulse generator whose on time is essentially constant over a single line cycle. Off time is terminated when current in the inductor falls to zero and the voltage on the side of the inductor not connected to the input voltage is less that the input voltage. A delay causes turn on to occur at the minimum of the voltage ring to minimize turn on switching losses. At voltages when the input voltage is less than one half of the output voltage part of the on time, turn on occurs with negative current flowing through the FET power switch and the inductor. Part of the turn on time is used to charge the inductor current back to zero before energy can begin to flow back into the output of the converter. A correction circuit is provided which extends the on time as a function of the input and output voltage to avoid dead time around the zero voltage crossover.

FIG.10

DOCUMENTS CONSIDERED TO BE RELEVANT

EP 93109938.6

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP - A - 0 223 316 (PHILIPS) * Column 5, line 8 - column 8, line 47; fig. 1; claims 1-4,7,8 *	1,3-6, 8,9	H 02 M 3/156 H 02 M 1/12 G 05 F 1/613 H 02 M 3/335
X	DE - A - 4 136 809 (MITSUBISHI DENKI K.K.) * Column 3, lines 22-60; column 7, line 57 - column 8, line 11; fig. 6; claims 1-3,5 *	1,3-6, 8,9	
Y	EP - A - 0 386 980 (THORN EMI) * Page 4, line 3 - page 5, line 15; fig. 4,5; claims 1-5,8,10,11 *	1,6,8, 9	
A		3	
Y	DE - A - 3 627 395 (PATENT-TREUHAND-GES.) * Column 7, line 45 - column 8, line 50; fig. 2; claims 1,2,9 *	1,6,8, 9	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 02 M G 05 F
A		5	
A	WO - A - 91/00 644 (HEWLETT-PACKARD) * Page 8, line 4 - page 10, line 21; fig. 2; claims 1,6,8,13 *	1,3,5, 6	
A	EP - A - 0 230 070 (SILICONIX) * Page 6, lines 1-18; fig. 5,6; claims 1,3,9,14 *	1,8,9	
A	DE - A - 3 838 408 (ANT NACHRICHTENTECHNIK)	1,3,8, 9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	11-10-1994	MEHLMAUER